Serial Number 09/252,243

Filing Date 14 January 1999

Inventor David R. Costa
Seth B. Suppappola

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Attorney Docket No. 78063

POWER ENVELOPE SHAPER

STATEMENT OF GOVERNMENT INTEREST

The invention described herein may be manufactured and used by or for the Government of the United States of America for Governmental purposes without the payment of any royalties thereon or therefor.

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The invention described herein relates to electronic circuits and their use in shaping power envelopes, and sonar systems making use of a shaped power envelope.

(2) Description of the Prior Art

It is known in the art to use pulsed (or gated) waveform in active sonar systems. These pulsed sonar systems may use signals that are continuous wave (CW), linear frequency modulated (LFM), stepped FM, etc. Often, two power levels are used: high power for long-range targets and low power for short-range targets. These predetermined power levels are used as the supply for the transmitter amplifier, which amplifies the gated signal and applies it to the transducer. Gating the transmit signal is equivalent to transmitting a signal with a square pulse envelope.

There are certain advantages, however, to transmitting a signal with a nonsquare-shaped envelope. For example, in the case of a gated sinusoid, the bandwidth of the transmitted signal is actually the bandwidth of the square pulse (a sinc function, in the frequency domain) centered about the frequency of the sinusoid. This gating results in sidelobes in the spectrum that are 13 dB down from the mainlobe. To reduce the sidelobes, it is necessary to shape the envelope of the transmitted sinusoid. In fact, sidelobes can be practically eliminated if a Gaussian-shaped envelope is used, but only at the expense of a wider mainlobe. Nevertheless, this condition may be desirable in certain applications.

When using a nontrivial shape for the envelope of a transmitted signal, signal generation becomes a more complex process than simple gating. One approach uses a low-level digital or analog electronics to generate the desired signal and its envelope, which is then applied to a linear power amplifier for application to the transducer. However, linear amplifiers are large, expensive, and inefficient. This inefficiency results in the internal dissipation of a considerable amount of power, which leads to massive heat transfer issues.

A need exists for a device which can efficiently provide control of a power envelope. Rapid switching, as well as low power loss, is required in order to generate a shaped power envelope efficiently.

SUMMARY OF THE INVENTION

It is an object of the invention to provide a power supply system having a shaped power curve.

It is a further object of the invention to provide a low power loss shaper for generating a signal.

It is a further object of the invention to provide a power envelope-shaping module, which may be adapted to existing sonar systems.

It is another object of the invention to provide a sonar system having a power envelope shaper using output transistors in two discrete states, either saturated or cut off.

Accordingly, the invention is a power envelope shaping device for joining to a serial control output. The device includes a power select circuitry module joined to the serial output. Multiple power switcher modules are joined to a plurality of incremental power sources and controlled by the power select circuitry module. In this way, each power switcher module can provide power from at least one of the incremental power sources on command from said power select circuitry module. The power switcher module outputs are joined together in order for providing varying power levels in accordance with a preprogrammed power envelope shape.

In a further embodiment, there is provided a sonar system comprising a computer for system control, a power envelope shaper, a transmitter module, and a transducer array. The power envelope shaper is comprised of three components, the power select

circuitry module, the power switcher module, and the battery pack. The power envelope shaper receives control signals from the system computer. These control signals, serial data and data clock, are processed by a power level decoder, which enables a selected output channel at the appropriate time. Each power switcher channel controls a single tap of the battery pack by enabling and disabling its output. If two or more taps are enabled at the same time, the highest voltage will prevail. The output power from the power switcher is fed directly to a sonar transmitter and controls the amplitude of the acoustic sonar signal. The topside computer provides the serial data control signals to the power switcher, using fast switching speeds throughout a plurality of channels, thereby allowing for the production of different sonar envelope shapes. The device as configured produces a Gaussian-shape with reduced side lobes.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing objects and other advantages of the present invention will be more fully understood from the following detailed description and reference to the appended drawings wherein:

FIG. 1 is a block diagram of the sonar system with a power envelope shaper.

FIG. 2 is a block diagram depicting a single output channel of the power switcher.

FIG. 3 is a block diagram of the complete power switcher circuit.

FIG. 4 is a graph depicting a Gaussian-shaped sonar pulse produced by the system.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. 1, the sonar system, designated generally by the reference numeral 10, is depicted in a block diagram showing its major components. A topside computer 12 controls the system by underwater cable 14 that is connected to the power envelope shaper module 16, the shaped power envelope 18 is outputted to the sonar transmitter 20 which, in turn, powers the transducer array 22. The result is a shaped sonar signal 24 having particular characteristics, such as reduced sidelobes, depending on the transmitted shape. The transmitted shape is determined by the power select circuitry 26 and the power switcher 28 located within the power envelope shaper 18. A multi-tap battery pack 30 provides power to the power switcher 28 to form the power envelope shape. The power envelope shaper 16 may be used with an existing sonar transmitter and transducer array to form a sonar signal envelope shaper. The power envelope shaper 16 is a self-contained, high speed, high power, efficient, power amplitude shaping device. The topside computer 12 digitally controls the power envelope shaper which outputs a preprogrammed arbitrary power envelope. This computer is preferably built on a VersaModule Eurocard (VME) chassis having a

serial output port; however, other commonly available computers can be used.

The power envelope shaper can be used by existing sonar transmitters and arrays to produce a shaped sonar waveform. The transmitter and transducer package in the preferred embodiment has a common ground wired to the case in several locations, thereby requiring the use of a high-side driver for the power switcher. A high-side driver is one in which the supply power is switched before reaching the load, whereas, a low-side driver is one in which the supply power is switched between the load and the supply ground.

A more detailed view of the power envelope shaper 16 may be seen in FIG. 2, which shows a single channel 80 of the multiple channel power envelope shaper 16. A TTL and Complimentary Metal Oxide Semiconductor (CMOS)-compatible MOS gate driver 32 used to switch the power-gating device 34. As discussed previously, MOS gate driver 32 must be a high side driver. Accordingly, gate driver 32 provides a differential output voltage. Gate driver 32 must also provide high input and output currents in order to turn power-gating device 34 on and off because of the high capacitance of the power-gating device 34. MOS gate driver 32 is preferably an International Rectifier IR2125™. Gate driver 32 uses a bootstrap or floating supply technique in which capacitor 36 is charged through diode 38 and keeps the power gating device 34 gate fifteen volts above the emitter voltage when the power gating device 34 is on. This floating supply technique is well known and

widely used and is very effective in high-side switching designs. Diode 38 is a fast recovery diode, so that capacitor 36 does not discharge. Capacitors 40 and 42 are bypass capacitors required to supply the transient current needed for refreshing the bootstrap supply. Capacitor 44 is a despiking capacitor used to suppress switching transients when the error output of gate driver 32 is not used. Diode 72 and diode 48 are fast turn-on diodes that protect the gate driver 32 by suppressing negative voltage transients. These voltage transients are caused by flyback current that is produced when switching an inductive load. The voltage V across an inductor L follows the relation:

$$V = L\frac{di}{dt} \qquad (1)$$

where di/dt is the time derivative of current flow through the inductor.

In this circuit, flyback current flows from ground 50 back to the high power supply, VIN 52, when the power gating device 34 turns off. This negative traveling current causes large negative voltage spikes. The metal oxide varistor (MOV) 54 and diode 56 protect the power gating device 34 collector-emitter junction from inductive flyback, in the same way that varistor 58 protects the gate-emitter junction. Zener diode 60 clamps positive transients above the Zener breakdown voltage of 5.1 V. Resistor 62 and resistor 64 limit the switching speed of the power gating device 34, resulting in slower turn-on and turn-off. This also results in a decrease in unwanted flyback, because di/dt in equation (1)

is reduced. Resistance of resistors 62 and 64 can be decreased if faster switching is required, but only at the expense of larger flyback transients. The fast turn-on diode 66 helps clamp negative voltage transients at the power gating device's emitter. Capacitor 68 is the bypass capacitor for the high-power supply. Diode 70 isolates each battery output from the others, while a fast turn-on diode 73, isolates each switching block from the others. The diode 73 is necessary so that the outputs of each switching block can be hard-wired together. In this configuration, the highest enabled output 74 will prevail. Power-gating device 34 must have a rise time of at most 49 ns and a fall time of at most 410 ns. An insulated gate bipolar transistor (IGBT) with high-power capabilities and a typical turn-on time of 43 nanoseconds was selected to fulfill these requirements for the power-gating device 34. MOSFET circuitry was initially tried for the power gating device 34, but the circuitry was unable to handle the high current requirements. The insulated gate bipolar transistor is preferably an International Rectifier IRGPC50F™. Each power switcher channel is capable of 70 Amperes of continuous current, a 600V breakdown voltage, and a maximum internal power dissipation of 200 Watts. High efficiency and a small package size are made possible because the IGBTs are operated in either the saturation or cutoff region. The operation allows for a minimal internal power dissipation and necessitates only small heat sinks. In the preferred embodiment,

a TO-247 heat sink with one-inch fins was used to dissipate heat from the power-gating device 34.

The complete power envelope shaper is shown in FIG. 3 including the field programmable gate array (FPGA)-based power level decoder (power select circuit 26), multi-tap battery pack 30, and each power-switcher channel 80. (For clarity only part of the channels and battery numerals are shown, each repeating in the array.) The control signals, serial data 82 and data clock 84 are processed by the power level decoder 26 which enables each power switcher channel 80 at the appropriate time. Each power switcher channel 80 controls a single tap of the battery pack 30 by enabling and disabling its output. A power envelope is produced by switching each battery tap at the appropriate time to generate the desired power waveform. The output power 86 from the power switcher 80 is fed directly to a sonar transmitter and controls the amplitude of the acoustic sonar signal. The desired sonar signal shape for this application was a Gaussian envelope, although the envelope shaper is versatile enough to produce an envelope of arbitrary shape.

FIG. 4 shows the Gaussian acoustic sonar signal that was produced. The shape and duration of the pulsed signal is digitally controlled by topside computer 12, which transmits a serial digital word via an underwater cable to a wet-side power level decoder 26. The serial word is decoded by an FPGA-based power level decoder, which generates the eleven enable signals that control each power switcher 80. To produce a Gaussian

envelope, the eleven discrete power levels were enabled sequentially and then disabled in a descending order. The transmitter uses this power to produce a pulsed sonar signal resulting in the Gaussian envelope 88.

The features and advantages of the invention are numerous. The computer control allows for fast switching speeds and the generation of virtually any power envelope shape. The power envelope shaper described above was developed as a separate underwater module, which may be used with an existing sonar transmitter in order to shape the envelope of a pulsed sonar signal. The use of discrete states wherein transistors operate only in the saturated or cut-off modes provide high efficiencies and minimum internal heat generation.

It will be understood that many additional changes in the details, materials, steps and arrangement of parts, which have been herein described and illustrated in order to explain the nature of the invention, may be made by those skilled in the art within the principle and scope of the invention.

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POWER ENVELOPE SHAPER

ABSTRACT OF THE DISCLOSURE

A power envelope shaping device for joining to a serial control output is disclosed. Multiple power switcher modules are joined to a plurality of incremental power sources and controlled by the power select circuitry module. In this way, each power switcher module can provide power from at least one of the incremental power sources on command from said power select circuitry module. The power switcher module outputs are joined together in order for providing varying power levels in accordance with a preprogrammed power envelope shape.

In a further embodiment, there is provided a sonar system comprising a computer for system control, a power envelope shaper, a transmitter module, and a transducer array. The power envelope shaper receives control signals from the system computer. These control signals, serial data and data clock, are processed by a power level decoder, which enables a selected output channel at the appropriate time. Each power switcher channel controls a single tap of the battery pack by enabling and disabling its output. The output power from the power switcher is fed directly to a sonar transmitter and controls the amplitude of the acoustic sonar signal. The computer provides the serial data control signals to the power switcher, using fast switching speeds thereby

allowing for the production of different sonar envelope shapes. The particular envelope shape may be immediately modified by software to produce Gaussian or other power envelope shapes.

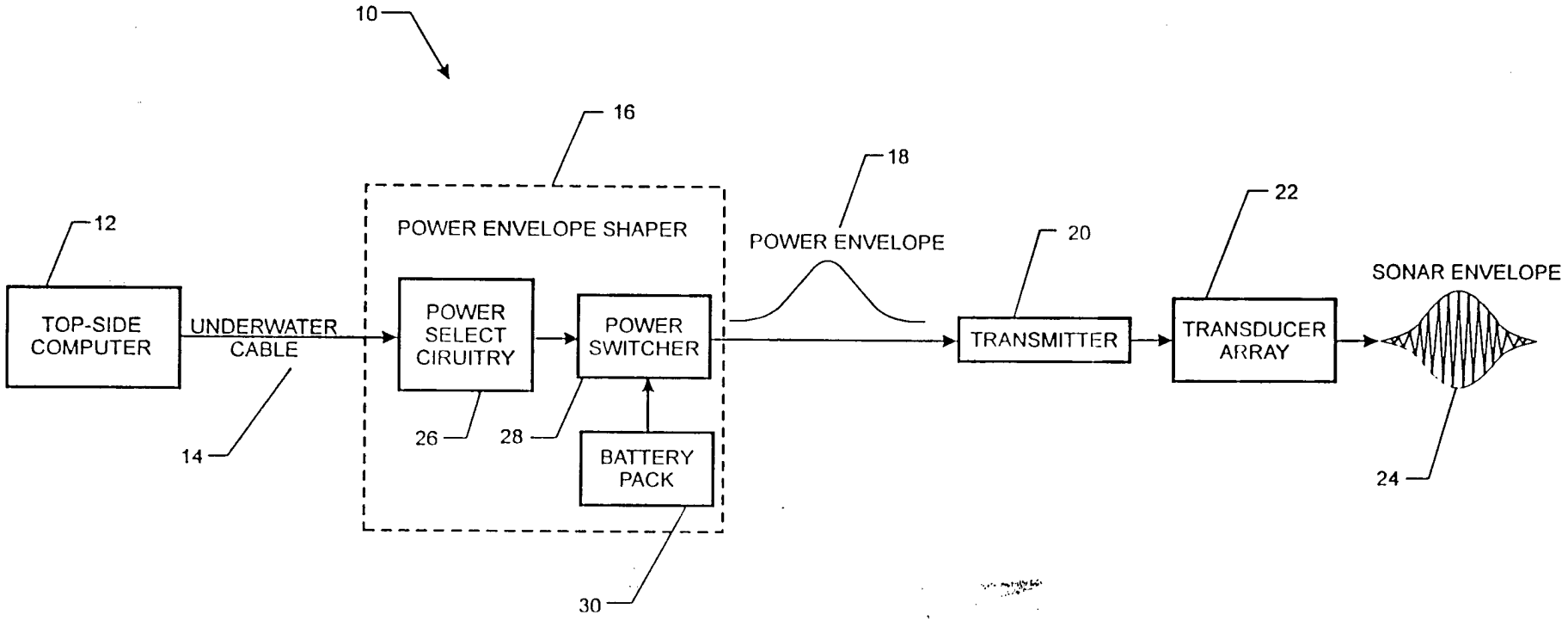
10
16
18
22
12
POWER ENVELOPE SHAPER
POWER ENVELOPE
20
SONAR ENVELOPE
TOP-SIDE COMPUTER
UNDERWATER CABLE
POWER SELECT CIRUITRY
POWER SWITCHER
TRANSMITTER
TRANSDUCER ARRAY
14
26
28
BATTERY PACK
24
30

FIG. 1

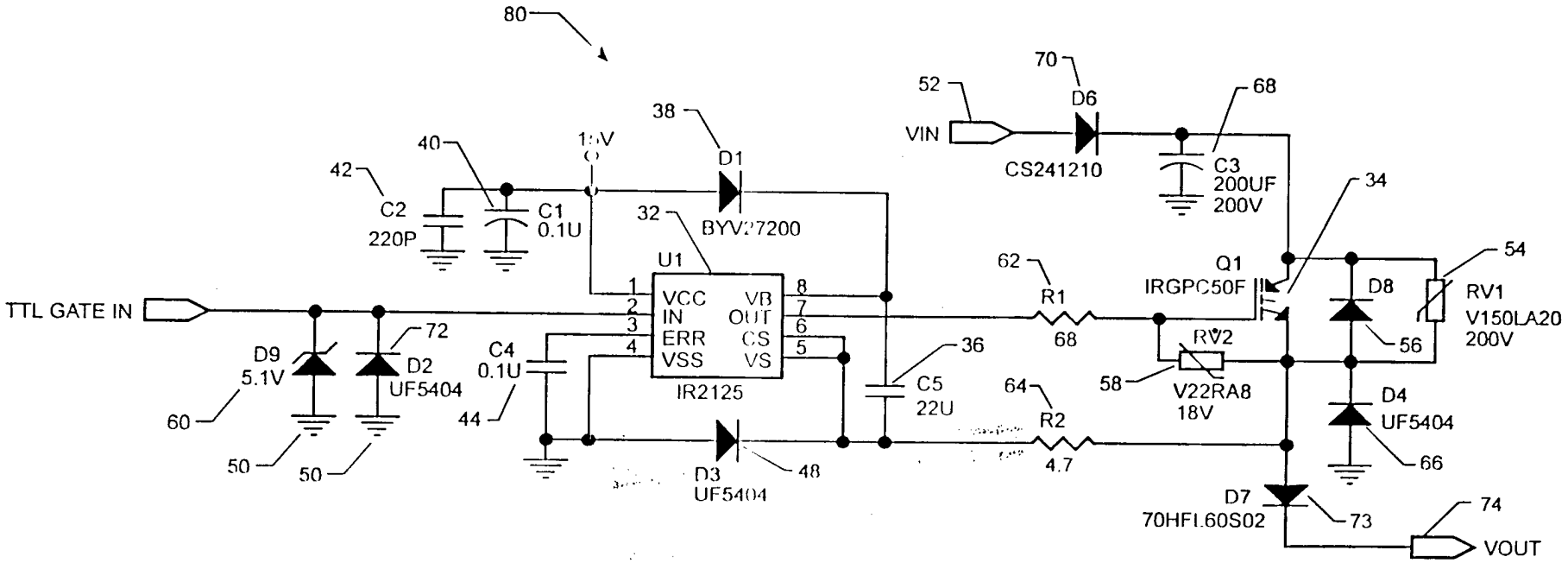
80
70
52
D6
68
38
VIN
CS241210
C3
200UF
200V
34
40
D1
42
C2
220P
C1
0.1U
32
BYV27200
U1
54
62
Q1
IRGPC50F
D8
RV1
V150LA20
200V
TTL GATE IN
1 VCC
2 IN
3 ERR
4 VSS
8 VB
7 OUT
6 CS
5 VS
IR2125
R1
68
RV2
V22RA8
18V
56
58
72
D9
5.1V
D2
UF5404
C4
0.1U
36
C5
22U
64
R2
4.7
D4
UF5404
60
44
50
50
D3
UF5404
48
66
D7
70HFL60S02
73
74
VOUT

FIG. 2

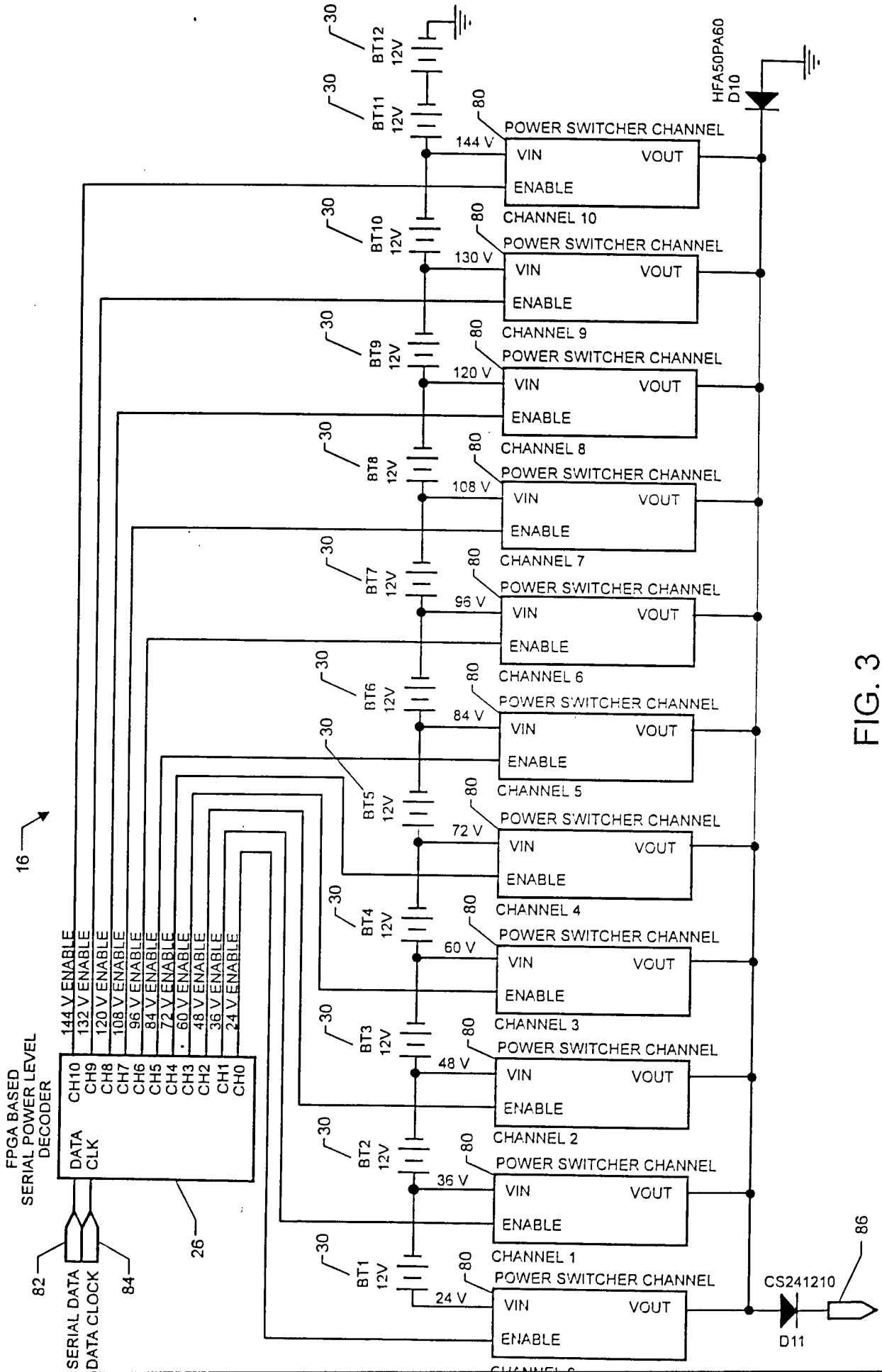
16
FPGA BASED SERIAL POWER LEVEL DECODER
DATA
CLK
CH10
CH9
CH8
CH7
CH6
CH5
CH4
CH3
CH2
CH1
CH0
144 V ENABLE
132 V ENABLE
120 V ENABLE
108 V ENABLE
96 V ENABLE
84 V ENABLE
72 V ENABLE
60 V ENABLE
48 V ENABLE
36 V ENABLE
24 V ENABLE
26
82
84
SERIAL DATA
DATA CLOCK
30
BT12 12V
BT11 12V
BT10 12V
BT9 12V
BT8 12V
BT7 12V
BT6 12V
BT5 12V
BT4 12V
BT3 12V
BT2 12V
BT1 12V
80
POWER SWITCHER CHANNEL
VIN
VOUT
ENABLE
144 V
130 V
120 V
108 V
96 V
84 V
72 V
60 V
48 V
36 V
24 V
CHANNEL 10
CHANNEL 9
CHANNEL 8
CHANNEL 7
CHANNEL 6
CHANNEL 5
CHANNEL 4
CHANNEL 3
CHANNEL 2
CHANNEL 1
HFA50PA60
D10
CS241210
D11
86
TRANSMITTER POWER

FIG. 3

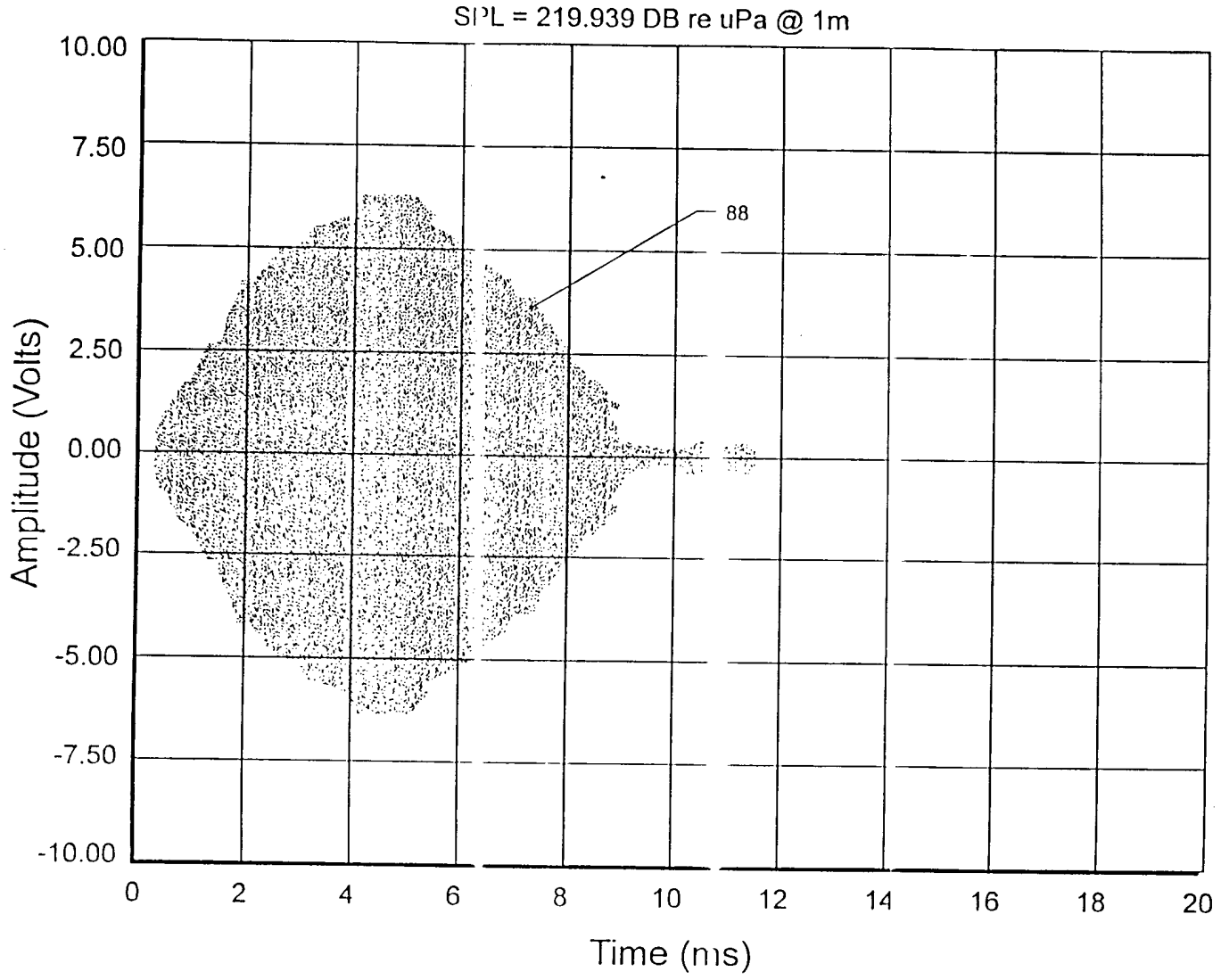
SPL = 219.939 DB re uPa @ 1m
10.00
7.50
5.00
2.50
0.00
-2.50
-5.00
-7.50
-10.00
Amplitude (Volts)
88
0
2
4
6
8
10
12
14
16
18
20
Time (ms)

FIG. 1